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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/795,825
Filing Date: March 08, 2004
Appellant(s): AFGHAHI ET AL.

John A. Wiberg
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 11/22/10 appealing from the Office action mailed on 6/22/10.

(1) Real Party in Interest

The examiner has no comment on the statement, or lack of statement, identifying by name the real party in interest in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

U.S. Patent No. 5,477,481 (Kerth) issued on 12/19/95

(9) Grounds of Rejection

Claims 9 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Kerth, U.S. Patent No. 5,477,481.

As to claim 9, note Fig. 4A of Kerth, where the step of

"sampling a voltage present at an input node" reads on the operation when the voltage at the top input terminal (where VINP is received) is transferred to the left plate of the top capacitor C1, i.e., when the top switch phiA closes; the step of "holding the sampled voltage at a reference node" reads on the storage of charge on the top capacitor C1 in response to the top switch phiA and the other phiA switch connected to the right plate of C1 closing; the recited step of "measuring an input signal at the input node by sampling the input signal and comparing it to the reference voltage" reads on the operation when the phiA switches open and the phiB switches close (note that this operation occurs at a predetermined interval after the sampling and holding of the voltage by switches phiA, and note that the input signal VINP gets compared to the reference voltage via comparator 48).

As to claim 10, the recited step of "activating a sampling circuit a predetermined interval before measurement of the input signal is initiated" reads on the closing of the phiA switches.

(10) Response to Arguments

Appellant argues that "when the [phiA] switch opens, the terminal receiving VINP (which the Examiner deems to be the

input node per claim 9) is cut off from the rest of the circuit. Therefore, the opening of the [phiA] switch cannot constitute measuring the input signal (VINP) at the input node by sampling the input signal and comparing it to the reference voltage, per claim 9. Also, closing the [phiB] switch admits the signal that existed at the right side of capacitor C1 to the + terminal of the differential chopped amplifier 48, but in no conceivable way does that result in a comparison of that signal to the VINP signal present at the input node. Even if the opening of the [phiA] switch did not cut off the input signal VINP from the rest of the circuit (it does), at best the result would be a serial provision of successive signals to the + terminal of the differential chopped amplifier 48, which obviously does not result in a comparison of such successive signals."

This argument is not persuasive because it appears to be based on a misunderstanding of the examiner's grounds of rejection. As noted above, in Fig. 4A of Kerth the step of "sampling a voltage present at an input node" in claim 9 reads on the operation when the voltage at the top input terminal (where VINP is received) is transferred to the left plate of the top capacitor C1, i.e., when the top switch phiA closes; the step of "holding the sampled voltage at a reference node" reads on the storage of charge on the top capacitor C1 in response to

the top switch phiA and the other phiA switch connected to the right plate of C1 closing; the recited step of "measuring an input signal at the input node by sampling the input signal and comparing it to the reference voltage" reads on the operation when the phiA switches open and the phiB switches close. Note that this operation occurs at a predetermined interval after the sampling and holding of the voltage by switches phiA, and note also that the input signal VINP gets compared to the reference voltage via comparator 48 (i.e., when switches phiB close, the sampled and held voltage on the top capacitor CI gets applied to the non-inverting input terminal of comparator 48 and the input signal VINP gets applied to the inverting input terminal of comparator 48). Also note that the recited step of "activating a sampling circuit a predetermined interval before measurement of the input signal is initiated" in claim 10 reads on the closing of the phiA switches.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

(12) Conclusion

For the foregoing reasons, it is respectfully submitted that the above-noted rejection of claims 9 and 10 based on Kerth is proper and therefore should be sustained.

Respectfully submitted,

/Kenneth B. Wells/
Primary Examiner
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Conferees:

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